With respect to the prior art rejections, claims 1-8, 10-13 and 23-38 stand rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 28-31 of Ajmera et al. (U.S. Patent No. 6,503,833 B1). Claims 1-8, 10-13, and 23-38 stand rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-50 of Cabral, Jr., et al. (U.S. Patent No. 6,444,578 B1). Finally, the Examiner indicates that claims 1-8, 10-13, and 23-38 appear to conflict with claims 1-30 of parent application No. 09/569,306.

Further, claims 1-3, 23, 4-6, 8, 12, 24, 13, 25 and 26 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Maa et al. (U.S. Patent No. 5,830,775). Claim 7 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Maa in view of Kanamori (Patent Application Publication US 2002/0009856 A1). Claims 10, 31 and 32 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Maa in view of Cabral, Jr., et al. (U.S. Patent No. 5,828,131).

These rejections are respectfully traversed in view of the following discussion.

Attached hereto is a marked-up version of the changes made to the claims by the current Amendment.

It is noted that the claim amendments herein are made only for more particularly pointing out the invention for the Examiner, and not for distinguishing the invention over the prior art, narrowing the claims, or for any statutory requirements of patentability.

Further, it is noted that, notwithstanding any claim amendments made herein, Applicant's intent is to encompass equivalents of all claim elements, even if amended herein or later during prosecution.

I. THE CLAIMED INVENTION

Applicant's invention, as exemplarily disclosed and claimed (e.g., see independent claim 1), is directed to a method for fabricating a silicide for a semiconductor device, which includes depositing a metal containing silicon or a metal alloy on a silicon substrate, reacting the metal containing silicon or the metal alloy to form a first silicide phase, etching any unreacted metal

containing silicon, depositing a silicon cap layer over the first silicide phase, reacting the silicon cap layer to form a second silicide phase, for the semiconductor device, and etching any unreacted silicon from the silicon cap layer.

Independent claims 4, 10, 13, 25, and 26 recite somewhat similar methods, but with some different limitations.

With such features and as mentioned previously, a reaction of a metal (e.g., Co in an exemplary embodiment, but other metals will be similarly operable as claimed and as clearly described in the specification) containing silicon or a metal alloy, to initially form Co_2Si, minimizes the silicon consumption of the thin SOI film (or bulk silicon) substrate.

The consumption of the thin SOI film is additionally reduced by the deposition of a silicon (or poly-silicon in a non-limiting exemplary variation of the invention) film on the Co_2Si.

Such exemplary features are not taught or suggested by any other prior art of record, either alone or in combination.

II. THE 35 U.S.C. §112, FIRST AND SECOND PARAGRAPH, REJECTIONS

While Applicant submits that specification clearly describes the claimed subject matter in a clearly enabling way, to allow one of ordinary skill in the art to make and use the invention, and while Applicant further submits that the claims are clear to one of ordinary skill in the art to recognize the metes and bounds of the invention, to speed prosecution, claims 5-8, 27, 29, 31, 33, 35 and 37 have been amended in a manner believed fully responsive to the Examiner's criticisms.

With regard to claims 23-24, Applicant notes the recitation of a "first silicide phase" and a "second silicide phase" in the claim is just a way to label the two different phases that form in the process.

In complete and fundamental contrast, the "first forming silicide phase" is the first in a sequence of a plurality of possible silicide phases that form when the metal reacts with Si. Typically, the "first forming" phase is also the most "metal-rich" phase.

Referring now to the conventional salicide process, when the wafer is annealed (e.g., the first rapid thermal anneal (RTA)), the first phase is CoSi. However, CoSi is not the first forming silicide phase. That is, the first forming silicide phase is Co_2Si. Since the first RTA anneal temperature is typically about 520°C, the second forming phase, CoSi is obtained, which Applicant "labeled" a first phase.

Thus, claims 23-24 are believed to be clear and sufficiently definite to one of ordinary skill in the art to know the metes and bounds of the invention.

In view of the foregoing, reconsideration and withdrawal of this rejection are respectfully requested.

III. THE PRIOR ART REJECTIONS

A. The §102(b) Rejection Based on Maa et al.

Regarding the rejection of claims 1-3, 23, 4-6, 8, 12, 24, 13, 25 and 26, Maa et al. (U.S. Patent No. 5,830,775) is clearly deficient.

First, it is noted that the Examiner clearly admits (e.g., see Item No. 10 on page 6 of the Office Action, etc.) that Maa et al. fails to teach or suggest "*a metal alloy or metal alloy containing silicon was deposited to form the silicide*". As the Examiner well-knows, for a §102 rejection, all limitations in the claim must be found, explicitly or inherently, within the four corners of a single reference. Here, Maa fails.

Independent claims 1, 4, 25, and 26 each clearly require a "metal containing silicon or a metal alloy..." (emphasis Applicant's). Thus, on its face, the Examiner's rejection is flawed.

Maa does not teach or suggest the use of a metal-silicon alloy or a metal alloy as silicidation material. Indeed, Maa teaches away from such a claimed feature.

Maa defines a "silicidation material" as one of pure metals such as "Co, Ti, Ni, W, Pt, Pd, Mo and Ta" (e.g., see Col. 4, line 63 of Maa). Maa suggests the use of a multi-layer stack "*[l]ayer 80 is either a uniform layer of a single metal, for example cobalt, or alternatively, is*

made up of more than one layer of silicidation material. For example, layer 80 might include a lower layer of Ti and upper layer of Co." (e.g., see Col. 4, line 64 to Col. 5, line 1 of Maa et al.). Maa does not suggest the use of a metal-silicon alloy. In fact, Maa does not propose, teach, or suggest the use of any alloys such as metal alloys, but rather clearly teaches that a layered structure of metals is desirable.

Thus, independent claims 1, 4, 13, 25, and 26, which clearly recite depositing "*a metal alloy or metal containing silicon*" are clearly not taught or suggested by Maa et al., and thus are clearly patentable over Maa et al., either alone or in combination.

Regarding dependent claims 2, 3, 5, 6, 8, 12, 23, 24, 27-30, and 33-38, these claims are patentable not only by virtue of their dependency from the above indpend3ent claims, but also for the additional limitations which they recite.

That is, first, with regard to dependent claims 23 and 24, Maa does not teach the use of a first forming phase as in the claimed invention.

Maa admits, in the disclosure thereof, that "*the compound form in 90 in Fig. 5 may contain both Co_2Si and CoSi*" (col. 5, line 30), with the reason being the narrow temperature window in which this first forming phase exists. This is precisely why Maa's disclosure avoids the term "metal-rich phase" when referring to 90 and instead named 90 as a "silicon deficient silicide".

Even assuming arguendo that Maa realized that it is preferable to form Co_2Si rather than CoSi to reduce silicon consumption form the substrate (Col. 5, lines 49-52), Maa only discusses the "likelihood of forming Co_2Si being improved if the temperature range is between 450C to 500C" (Col. 5, lines 55-57). However, Maa provides no sound method by which only Co_2Si is obtained from such a process. Indeed, Maa avoids the term "metal-rich phase" and uses the term "silicon deficient silicide".

Thus, Maa merely mentions that Co_2Si may be preferable, but teaches or suggests no method of getting there, and certainly not with the clear, unique, and unobvious combination of process steps of the present invention.

In essence, even if Maa may realize the it is preferable to form Co_2Si (a metal-rich phase),

Maa is merely indicating that "it would be nice to do this, but I don't know how to do it". Maa teaches no method for obtaining Co_2Si. He merely discloses that there may be an incidental chance of obtaining Co2Si (presumably if many hundreds (or thousands) of wafers are processed) and that such would be preferable over CoSi. However, merely indicating that something is preferable does not teach <u>how</u> to achieve the metal-rich phase

In complete and fundamental contrast, the claimed invention has clear process steps utilizing <u>a metal containing silicon or a metal alloy</u> as a way to obtain, for example, Co_2Si (and as defined in some of the present claims, as the "first forming phase").

Moreover, the incorporation of silicon into the metal reduces further the silicon consumption from the wafer already at the formation of the Co_2Si phase. None of these exemplary features is taught or suggested by Maa.

The Examiner's position regarding Maa depositing a "metal alloy" is <u>clearly erroneous</u>.

Indeed, referring to page 4 of the Office Action, Applicant points out that Maa does not deposit a metal alloy layer 80, but instead <u>deposits a pure metal layer or a stack of pure metals</u>. Maa does not teach or suggest forming a first metal rich silicide 90, but instead teaches a "silicon deficient silicide" that is "a phase of silicide having proportionally less silicon and more silicidation material than the more stable disilicide phase silicide" (see column 5, lines 14-16 of Maa; see also claim 1 of Maa).

Additionally, regarding dependent claims 28, 30, 34, 36, and 38, the Examiner assert on page 5 of the Office Action that "*[r]egarding claims 28, 30, 34, 36, and 38 it is seen to be inherent that the metal-alloy extends the temperature window in which a silicide metal-rich phase exist ... In other words, the more metal that is present relative to silicon the longer the window. Consequently if an alloy absent silicon is used the window is larger then if silicon is present.*"

However, Applicant respectfully submits that this is clearly incorrect.

Based on the above passage, the role of the silicon in the metal-containing silicon, does not appear to be understood or appreciated. <u>The addition of silicon to the metal widens the temperature window.</u>

Thus, the Examiner's statement on page 5 of the Office Action that "in other words, the more metal that is present relative to silicon, the longer the window", is clearly incorrect. Indeed, it is just the opposite. Adding silicon widens the window, not shortens it.

Referring to the exemplary case of cobalt-silicon alloy, an alloy absent of silicon result in a window that is only 20 °C wide. With the addition of 20% silicon, thus forming a Co(0.8)-Si(0.2) alloy, the window opens up and is 100°C wide. This is a major benefit of the invention, and is not at all appreciated by Maa..

Therefore, the use of a metal containing silicon or a metal alloy is important for obtaining the first forming phase Co_2Si. Such is no taught or suggested anywhere within Maa et al.

B. The §103(a) Rejections Based on Maa et al. In view of Kanamori, or Cabral et al.

Regarding the rejection of claim 7 based on Maa in view of Kanamori (Patent Application Publication US 2002/0009856 A1), and the rejection of claims 10, 31 and 32 based on Maa in view of Cabral, Jr., et al. (U.S. Patent No. 5,828,131), even assuming arguendo that Kanamori and/or Cabral et al. would have been combined with Maa et al., Kanamori and Cabral et al. clearly fail to make up for the above deficiencies of Maa et al.

Indeed, Kanamori discloses a method of fabricating a semiconductor device self-aligned silicide areas formed using a supplemental silicon overlayer. Such methods are completely and fundamentally different from that of the invention defined by dependent claim 7.

Again, the claimed invention defined by claim 7 (and its dependency from independent claim 4) is clearly distinguished from Maa and Kanamori by the use of a metal alloy or a metal containing silicon (e.g., Co_xSi_{1-x}; a metal-silicon mixture), rather than a pure metal. The use of the alloy encapsulates two important advantages of the claimed invention, which are not shared by Maa and/or Kanamori, as discussed above.

First, the metal-silicon mixture already contains some of the silicon required to form the silicide. Thus, less silicon is consumed from the substrate during the subsequent anneal. Indeed, none of the references teaches or suggests using such a metal-silicon mixture, let alone for the

reason and purpose of the invention.

Secondly, alternatively, a metal alloy may be deposited instead of the metal-silicon mixture. The term "metal alloy" means a metal and another material (e.g., another metal, a semiconductor, etc.). Using such a metal alloy allows many benefits (e.g., enables applying the silicon cap to the very first forming phase (e.g., Co_2Si), rather than a later phase (e.g., CoSi)).

Furthermore, as noted in the previous Amendment and as mentioned above, the use of the metal-silicon mixture is fundamental to the inventive method and is neither taught or suggested by Maa et al. and/or Kanamori. Indeed, referring to the diffraction maps shown in Figures 2A and 2B of Exhibit I submitted with the Amendment on May 14, 2002, the top map (e.g., Figure 2A) shows the evolution of the Co-silicide phases when pure Co metal is used (as opposed to a metal containing silicon or an alloy, as in the claimed invention).

At a temperature lower than about 440 °C, no reaction takes place, and only pure Co is measured. Then, when the temperature is increased, the Co_2Si phase forms and exists only within a narrow window of about 20 °C, after which the phase changes into CoSi.

The CoSi phase persists up to 625 °C where it changes into $CoSi_2$. Since the Co_2Si phase only exists in a very narrow, tight temperature window, it is very difficult to form (e.g., very unreliable and prone to error or being missed based on nonuniform doping of the substrate, etc.), and, in practice, the later phase (e.g., CoSi) is used in self-aligned silicide processes.

The bottom map (e.g., Figure 2B) shows the evolution of reacting a metal (e.g., Co) containing silicon or a metal alloy, as in the claimed invention.

That is, Figure 2B shows the metal (e.g., Co)-silicide phases when a Co-silicon mixture having 20% silicon is used instead of pure Co. In this case, the Co_2Si phase exists over a large temperature window of more than 100 °C. This makes it possible to practice a self-aligned silicide process where the first phase is also the first forming phase (Co_2Si). As a result, much more reliable and easier manufacturing processes are possible since it is easier to stop on Co_2Si, etc. Then, annealing can be performed, etc. to go to CoSi, and finally to $CoSi_2$.

Again, Applicant submits that such is not trivial to use the method above (including using the metal-silicon mixture or a metal alloy), and thus, it is clear that Kanamori et al. does not

make up for the deficiencies of Maa.

Regarding the rejection of independent claim 10 (and claims 31 and 32), similarly, to Kanamori, Cabral et al. does not make up for the deficiencies of Maa et al. Cabral et al. is addressing the issue of the high temperature anneal required to form the low resistivity C54 phase, and proposes a method for lowering the formation temperature. It is noted that this issue is rather specific to titanium silicide and does not apply to all silicides in general.

Again, the $TiSi_2$ phase can exist in two polycrystalline structures.

The first polycrystalline structure (e.g., the C49 phase) has a resistivity of about 60-90 micro-ohm-cm. The second polycrystalline structure (e.g., the C54 phase) has a lower resistivity of about 12-20 micro-ohm-cm, and is therefore the desired phase. The C49 phase forms at about 650 °C. The C54 phase forms at a higher temperature of about 766 °C (See Fig 12 in Cabral). Such a high formation temperature can lead to device degradation, and agglomeration of the silicide film if a high enough anneal temperature is used to ensure the phase transformation for small circuit features.

Cabral et al. is addressing the issue of the high temperature anneal required to form the low resistivity C54 phase, and proposes a method for lowering the formation temperature. Again, it is noted that this issue is rather specific to titanium silicide and does not apply to all silicides in general.

Specifically, Cabral proposes depositing a Ti film over a refractory metal such as Ta, Nb, Mo, or W, and annealing to form a C54 $TiSi_2$ phase. In a different embodiment, Cabral deposits a Ti-Si alloy over the refractory metal. This alloy is targeted to be stoichiometric $TiSi_2$, but may be richer or leaner in its silicon composition (See column 6, lines 4-17).

First, Applicant submits that, given the disparate problems faced by each of Maa, Cabral and the present invention, it would not have made it "obvious" to combine the references, absent impermissible hindsight construction of the present invention, made possible only through a keyword search by the Examiner after a thorough reading of Applicant's own specification. Indeed, Cabral is trying to solve a different problem than Maa (let alone that addressed by the present invention as explained below).

Secondly, Cabral is not proposing a process which reduces silicon consumption. Cabral's proposes a method for forming the C54-$TiSi_2$ at a lower temperature than the conventional method, and preferably with one anneal.

Cabral (similarly to Besser) is silent with respect to forming any of the intermediate silicon-rich phases. When annealing Ti over silicon, the following phases form with increased temperature:

Ti -> Ti_3Si -> Ti_5Si_3 -> Ti_5Si_4 -> TiSi -> C49-$TiSi_2$ -> C54-$TiSi_2$.

In contrast to Cabral, following the method of the present invention, one would first form a silicon-rich phase, such as the Ti_5Si_3 phase, etch the unreacted Ti, apply a silicon cap, and then run a second anneal to form the C54-$TiSi_2$ phase.

Cabral does not teach or suggest forming the Ti_5Si_3 phase or any other intermediate phase, but actually proposes a method that forms the final phase C54-$TiSi_2$ in one annealing step. Indeed, Cabral attempts to avoid the second "conversion-anneal". His process will preferably have one anneal step that will form the C54 $TiSi_2$ phase (See for example, column 2, lines 23-30, and column 6, lines 22-26).

Additionally, the embodiment in which Cabral proposes using a near stoichiometric $TiSi_2$ alloy, cannot be applied to the self-aligned silicide (SALICIDE) method. The SALICIDE process includes applying a blanket metal film (such as Ti) onto a device structure (such as a MOSFET), annealing the wafer to react the metal with silicon surfaces to form a silicide (the metal over insulator surfaces, such as the MOSFET's sidewalls, does not convert into a silicide and remains a metal), etching the unreacted metal, and performing a second anneal to reach the desired silicide phase. The etching of the unreacted metal is essential to prevent bridging which otherwise will short the device source or drain area to the gate.

The above-described process is summarized in Cabral on column 1, line 47-55, and on column 11, line 48 to column 12, line 18. The etching is selective in the sense that it attacks the pure metal, but does not attack the silicide.

The SALICIDE process cannot be performed with a blanket deposited Ti - Silicon alloy

(as opposed to Ti alloy, which is defined in Cabral as Ti with some refractory metal) having a composition of stoichiometric $TiSi_2$, since the selective etch would no longer work. When a pure Ti or metallic Ti alloy is used, the metal over the device spacers does not convert into silicide during the anneal. Therefore, the unreacted metal can be etched since the etchant attacks only the metal, and does not remove silicide.

In contrast, when a near stoichiometric Ti-Silicon alloy is blanket deposited, the spacers are covered with a Ti silicide the same as the rest of the device surfaces and the selectivity of metal versus silicide is lost. It is noted that this is precisely one of the reasons that Cabral specifies the refractive metal for forming the Ti alloy as being "preferably a metal that is capable of forming a metal silicide" (column 3, lines 65-66). In addition, Cabral describes the application of his invention to the SALICIDE method only with Ti alloy (column 11, lines 48-65).

Cabral is "skipping" the intermediate silicide phases. In contrast, Applicants are using a metal alloy (or metal containing silicon) to extend the temperature window in which the silicide metal-rich phase exists. For example, this temperature window is extended from 20 °C to over 100 °C in the case of Co_2Si. This allows the invention to reliably form the metal-rich phase and apply the silicon cap as early as possible in the SALICIDE process. In complete and fundamental contrast, Cabral is trying to minimize the temperature window where the metal-rich silicide exists so that the final phase (C54-$TiSi_2$) will form at a lower temperature than that of the conventional method.

Thus, Applicants submit that Maa and Cabral would not have been combined by one of ordinary skill in the art at the time of the invention and absent hindsight.

Additionally, even assuming arguendo that Maa and Cabral would have been combined in the manner urged, the claimed invention would still not have been produced. Thus, claims 10 and 31-32 are patentable over the Examiner's proposed combination.

IV. THE DOUBLE PATENTING REJECTIONS

With respect to the double patenting rejections, claims 1-8, 10-13 and 23-38 stand

rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 28-31 of Ajmera et al. (U.S. Patent No. 6,503,833 B1).

However, Applicant has closely reviewed claims 28-31 of Ajmera et al. and submits that there are clear limitations found in claims 1-8, 10-13, and 23-38 which are not taught or suggested by claims 28-31 of Ajmera et al. Again, Applicant points out to the Examiner that for a double patenting rejection, only the claims of the applied patent can be relied upon, not the disclosure. The Examiner cannot imaginatively read into the claims, limitations found only in the disclosure of the applied patent. Thus, here there are limitations in claims 1-8, 10-13, and 23-38 which are not taught or suggested by Ajmera et al.

Claims 1-50 of Cabral, Jr., et al. (U.S. Patent No. 6,444,578 B1) are similarly deficient.

Finally, the Examiner indicates that claims 1-8, 10-13, and 23-38 conflict with claims 1-30 of parent application No. 09/569,306. However, claims 1-30 of the copending application have been reviewed and clearly do not conflict with the present claims. Indeed, different inventions are being prosecuted and specifically methods directed to different inventive steps. Thus, the claims of the present application do not conflict with claims 1-30 of the copending applications.

Notwithstanding the above, Applicant reserves the opportunity to file a Terminal Disclaimer at a later time.

In view of all of the foregoing, Applicant submits that all of the pending claims are patentable over the prior art of record.

V. FORMAL MATTERS AND CONCLUSION

In view of the foregoing, Applicant submits that claims 1-8, 10-13 and 23-38, all the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the

Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Assignee's Deposit Account No. 50-0510.

Respectfully Submitted,

Date: 6/13/03

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CERTIFICATION OF FACSIMILE TRANSMISSION

I hereby certify that I am filing this paper via facsimile, to Group Art Unit 2813, at (703) 872-9318, on June 13, 2003.

Respectfully Submitted,

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VERSION SHOWING MARKINGS MADE

IN THE CLAIMS:

5. (Amended) The method of claim 4, wherein said depositing of said metal containing silicon comprises performing a blanket deposition [of a], wherein said metal [comprising] comprises one of Co and Ti.

7. (Amended) The method of claim 6, wherein said blanket deposition is followed by a TiN cap deposition for preventing oxidation during a subsequent anneal processing.

8. (Amended) The method of claim 4, wherein said reacting of said metal containing silicon or said alloy comprises performing a first rapid thermal anneal (RTA) to form a metal-silicon phase, such that the deposited metal containing silicon with the [underlay Si] underlying bulk silicon substrate, converts some of the Si into metal-Si,

wherein said etching comprises selectively etching any unreacted metal, thereby leaving the metal-silicon regions intact,

wherein said depositing comprises performing a blanket deposition of a silicon film, and

wherein said reacting of said silicon cap comprises performing a second RTA to form a metal di-silicide.

27. (Amended) The method of claim 1, wherein said first silicide phase comprises a [silicon] metal-rich phase.

29. (Amended) The method of claim 4, wherein said first silicide phase comprises a [silicon] metal-rich phase.

31. (Amended) The method of claim 10, wherein said first silicide phase comprises a [silicon] metal-rich phase.

33. (Amended The method of claim 13, wherein said first silicide phase comprises a [silicon] metal-rich phase.

35. (Amended) The method of claim 25, wherein said first forming silicide phase comprises a [silicon] metal-rich phase.